

**VLSI PHYSICAL DESIGN: FROM GRAPH  
PARTITIONING TO TIMING CLOSURE**

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**Full text of "VLSI Physical Design\_ From Graph Partitioning to Timing Closure"**

Chapter 8 - Timing Closure. VLSI Physical Design: From Graph Partitioning to Timing Closure. Original Authors: Andrew B. Kahng, Jens Lienig, Igor L. Markov, .

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Topics routing, net, nets, placement, design, algorithm, timing, global, node, cell, global routing, clock tree, detailed placement, physical design.

VLSI Physical Design: From Graph Partitioning to Timing Closure introduces and compares algorithms that are used during the physical design phase of.

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The order of the blocks is typically chosen by a linear-ordering algorithm. The floorplanning stage ensures that 1 every chip module is assigned a shape and a location, so as to facilitate gate placement, and 2 every pin that has an external connection is assigned a location, so that internal and external nets can be routed.

The KL algorithm operates on a graph representation of the circuit, where nodes are gates and edges are nets. This is a non-trivial task - not only are poly and Metall mostly reserved for cells, but different layers have varying sheet resistances, which strongly affects timing characteristics. Compute the balance criterion. From Graph Partitioning to Timing Closure" introduces and compares algorithms. 5pp.